layer 205 of the first conductivity type. (Fig. 2 (D)).

In the Claims:

The following replacement claims are respectfully submitted:

1. (Amended) A method of manufacturing an LDMOS transistor comprising:

providing a semiconductor substrate of a first conductivity type having a well region of a second conductivity type formed on a surface thereof;

implanting ions of the first conductivity type into a part of the well region;

forming a gate oxide layer on the surface of the semiconductor substrate,

said forming a gate oxide layer including subjecting the semiconductor substrate to a heat treatment so that the implanted ions are diffused to form a diffusion region of the first conductivity type on the surface of the semiconductor substrate;

forming a gate electrode on the surface of the semiconductor substrate; and

forming a drain region on the surface of the semiconductor substrate,

wherein said implanting ions is carried out with an energy set so that an accelerated oxidation during said forming a gate oxide layer is inhibited.

3. (Amended) A method of manufacturing an LDMOS transistor according to claim 1, wherein the energy is about 500KeV.

5. (Amended) A method of manufacturing an LDMOS transistor according to

claim 1, wherein said implantation is conducted into a region of the semiconductor substrate where the drain region is formed.

7. (Amended) A method of manufacturing an LDMOS transistor comprising:

providing a semiconductor substrate of a first conductivity type having a first well region of a second conductivity type formed on a surface thereof, and a second well region of the first conductivity type formed within the first well;

implanting ions of the second conductivity type into a part of the second well region;

forming a gate oxide layer on the surface of the semiconductor substrate,

said forming a gate oxide layer including subjecting the semiconductor substrate to a heat treatment so that the implanted ions are diffused to form a diffusion region of the second conductivity type on the surface of the semiconductor substrate within the second well;

forming a gate electrode on the surface of the semiconductor substrate; and

forming a drain region on the surface of the semiconductor substrate,

wherein said implanting ions is carried out with an energy set so that an accelerated oxidation during said forming a gate oxide layer is inhibited.

9. (Amended) A method of manufacturing an LDMOS transistor according to claim 7, wherein the energy is about 500KeV.

11. (Amended) A method of manufacturing an LDMOS transistor according to claim 7, wherein said implantation is conducted into a region of the semiconductor substrate where the drain region is formed.

13. (Amended) A method of manufacturing an LDMOS transistor comprising:

providing a semiconductor substrate of a first conductivity type having a first well of a second conductivity type formed on a surface thereof within a first region, and a second well of the first conductivity type formed within a second region that is inside of the first region;

implanting ions of the second conductivity type into the second well;

forming a gate oxide layer on the surface of the semiconductor substrate,

said forming a gate oxide layer including subjecting the semiconductor substrate to a heat treatment so that the implanted ions are diffused to form a diffusion region of the second conductivity type located in a third region that is inside of the second region;

forming a gate electrode on the surface of the semiconductor substrate, the gate oxide layer extending from the first region to the third region through the second region; and

forming a drain region on the surface of the semiconductor substrate within the first region,

wherein said implanting ions is carried out with an energy set so that an accelerated oxidation during said forming a gate oxide layer is inhibited.

15. (Amended) A method of manufacturing an LDMOS transistor according to claim 13, wherein the energy is about 500KeV.

17. (Amended) A method of manufacturing an LDMOS transistor according to claim 13, wherein said implantation is conducted into a region of the semiconductor substrate where the drain region is formed.